S. L. Wong et al. (Eds.) (2010). Proceedings of the 18th International Conference on Computers in Education. Putrajaya, Malaysia: Asia-Pacific Society for Computers in Education.

Development of Pipeline Time Chart Tool for Microprocessor Design Education

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Abstract: We developed a pipeline time chart tool to explore pipeline control for microprocessor design education. Since the developed tool is not signal level but instruction level, the user of this tool can visually understand the microprocessor pipeline control. The user can set and run the pipeline control. Since the user can also modify the pipeline control flexibly, the user can examine the influence of the pipeline control change. Therefore, the user can learn good pipeline control of the microprocessor visually and effectively, and could get the design skill for thinking of the specification of pipeline control. This developed tool is very useful for students and young engineers.

Keywords: microprocessor design education, pipeline control, time chart

1. Introduction

Microprocessor design education becomes substantial. The design education of pipeline microprocessor in university is also coming [1]. The students usually practice implementing processor there. However the students do not think about meaning and effect of specification, because the specification of microprocessor is given to the students in conventional design education. We believe that the design skill for thinking of the specification is very important for microprocessor design education [2] [3]. This paper describes a pipeline time chart tool to get the design skill that is focused on the specification.

2. Pipeline Time Chart Tool

We developed a pipeline time chart tool to explorer pipeline control for microprocessor design education. The pipeline time chart tool is a component of the MEIji University Microprocessor design Education System (MEIMES). Time chart tools are usually used in computer design education. However, they are too difficult for student to understand computer architecture, because they are based on signal level. An instruction level based time chart is expected, but it is only seen in text books of computer architecture. Any time chart diagram in the book is not enough to learn the architecture of pipeline processor. Therefore, we developed time chart tool in instruction level for pipeline processor. Our proposed pipeline time chart tool does not exist so far. By using our time chart tool, students can visually understand execution of pipeline stage of each instruction, and flexibly change pipeline control for thinking the specification of pipeline processor.

Figure 1 shows overview of the developed pipeline time chart tool. The instruction set is COMET's. The COMET is a very- known virtual simple educational processor defined by Information-Technology Promotion Agency, Japan. The processor of Fig.1 has five-stage pipeline. Five stages are instruction fetch (IF), instruction decode (ID), operand fetch (OF), memory access (MEM), and execution in ALU and write back result (ALU). The area of the pipeline where the processor runs is colored with a proper color of the instruction. The user can visually understand execution of the pipeline stage of each instruction by our tool.

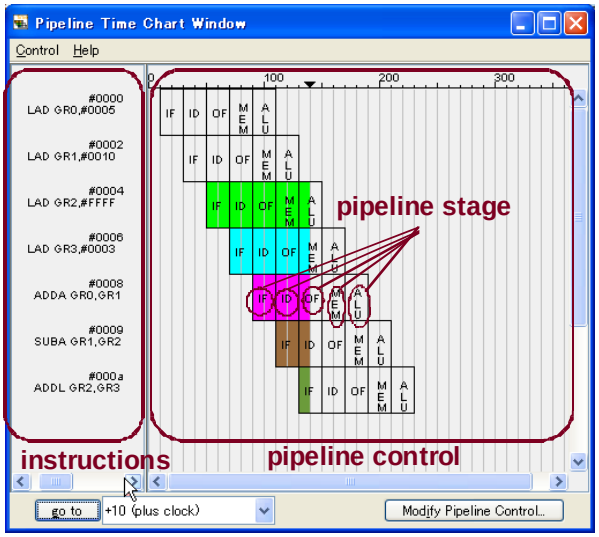

Figure 1 Pipeline time chart tool

The pipeline control of processor may cause three kinds of hazards. The pipeline time chart tool can indicate occurrence of all pipeline hazards. Figure 2 shows an example of structural hazard. The processor has only one memory and the LD instruction at address of #0000 accesses to the memory in MEM stage. Therefore, the SUBA instruction at #0005 cannot simultaneously accesses to the same memory in IF stage,. The pipeline hazard is displayed with a red arrow line between stages of the instruction where the problem occurs, and error or warning mark is attached with the instruction that does not give a correct result. When the user puts cursor on the mark, detail of the hazard is shown by tool tip. Figure 3 shows occurrence of data hazard. The ADDA instruction at #0004 cannot reads data of GR0 in OF stage, before the LD instruction at #0000 writes result to GR0 in ALU stage. Figure 4 shows the situation during executing branch instruction. Warning marks are attached at instructions after the branch instruction, because the processor does not know whether these instructions execute or not. If execution sequence of instruction is branched and branch hazard occurs, the warning marks are replaced with error marks as shown in Fig. 5. The pipeline time chart tool can also shows measures against pipeline hazards, such as data forwarding and pipeline flush, with blue arrow lines.

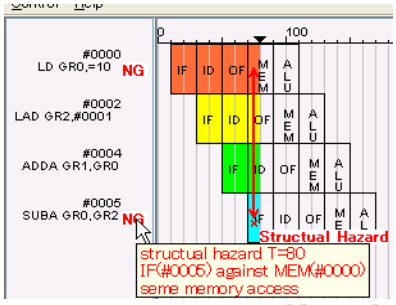

Figure 2 Structural hazard

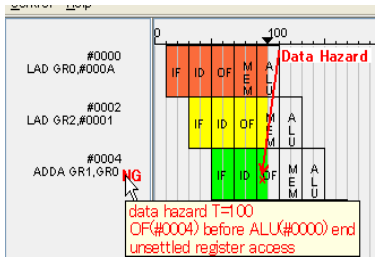

Figure 3 Data hazard

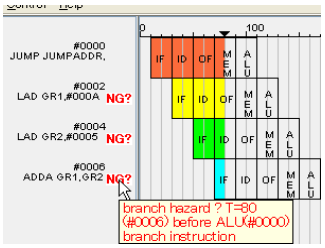

Figure 4 Executing branch instruction

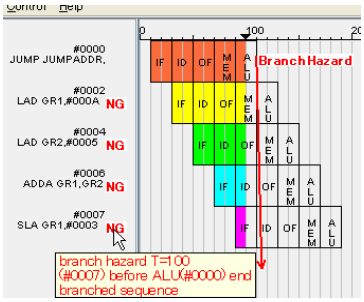

Figure 5 Branch hazard

The start time and processing time of each stage of the instruction are changeable with mouse dragging as shown in Fig. 6. The instruction which is specified with mouse is also cancelable. Therefore the users can flexibly modify the pipeline control, and then they can examine the influence of the pipeline control change. Figure 7 shows an example of avoidance of structural hazard of Fig.2. The structural hazard of Fig. 2 is resolved by waiting the IF stage of the SUBA instruction until memory access completion of the LD instruction in MEM stage.

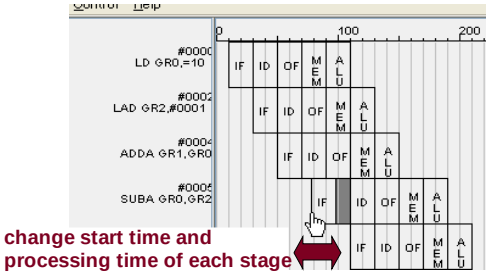

Figure 6 Modification of pipeline control

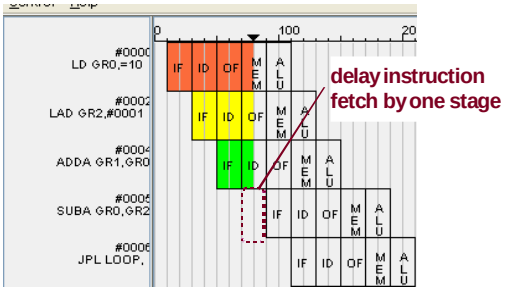

Figure 7 Avoidance of structural hazard

The users can explore combinations of instruction and stage with which the processor works correctly. They can learn good pipeline control of the microprocessor visually and effectively by using the pipeline time chart tool with a guide tool of MEIMES.

3. Conclusion

We developed the pipeline time chart tool to explore the pipeline control for microprocessor design education. The students and young engineers can learn meanings and effects of the specification in the pipeline control through examining the behavior of pipeline by using our tool. Therefore, the users could get the design skill for thinking about the specification of pipeline control architecture. This developed tool is very useful for students and young engineers. Learning using this tool is scheduled in computer architecture class of our university in 2010.

References

[1] Takahashi, R. & Ohiwa, H. (2003). Situated Learning on FPGA for Superscalar Microprocessor Design Education. Proc. SBCCI 2003 (pp.243-248). San Paulo, Brazil: IEEE Computer Society Press

[2] Morimoto, T & Tsutsumi, T.(2005). Early Development of Microprocessor Design Education System MEIMES-DESIGN. Proc. Forum on Information Technology 2005 (Vol.4 pp.353-354).Tokyo, Japan : ISPJ and IEICE (In Japanese)

[3] Morimoto, T & Tsutsumi, T. (2009). Development of Instruction Analysis Tool for Computer Design Education. Proc. The17th International Conference Computer In Education ICCE2009(pp.489-491). Hong Kong: APSCE